

Turnstile Operation Using a Silicon Dual-Gate Single-Electron Transistor

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A single-electron turnstile has been demonstrated using a silicon-based dual-gate single-electron transistor (SET). Each gate independently controls the closing and opening of the channel acting as the SET lead, which enables single-electron transfer synchronized with ac gate biases. By applying ac biases to the dual gates with a frequency f of ~ 1 MHz and a phase shift of π , current staircases quantized in units of ef are observed in drain current vs drain voltage characteristics at 25 K. [DOI: 10.1143/JJAP.42.L1109]

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The manipulation of elementary charge has been of great interest from the viewpoint of application to future integrated circuits and metrological standards. Methods enabling single-charge transfer in a time-correlated manner have been discussed since the very early stages of the single-electron device research,^{1,2)} and several devices are now available for this purpose. They are called single-charge transfer devices.^{3–7)} The single-electron turnstile^{3,4)} is one of them, and is based on the Coulomb blockade and the single-electron tunneling.^{8,9)} When we aim at its practical use, making it using silicon is quite preferable. This is because silicon-based single-electron-tunneling devices can operate at high temperatures,^{10–12)} and have high offset-charge immunity¹³⁾ and high controllability of gate capacitance^{10,11,14)} and threshold voltage.¹⁵⁾ Here, we report the first demonstration of a single-electron turnstile based on silicon.

The present turnstile relies not on multiple islands³⁾ but on a single island with multiple gates.⁴⁾ Figure 1 shows a scanning-electron-microscope (SEM) image and a schematic view of the device. The device is in effect a single-electron transistor (SET) with dual gates positioned over the island.¹⁶⁾ The dual gates have equal capacitive coupling to the island. They also couple to the lead of the SET, which enables us to control the electron density there. In other words, each SET lead is an independently controllable electron channel of an ultrasmall metal-oxide-semiconductor field-effect transistor (MOSFET).

With the dual-gate SET, we have already demonstrated a single-electron pump operation.¹⁷⁾ The single-electron pump belongs to the same class of charge transfer device as the turnstile. The pump uses in its operation two adjacent Coulomb blockade states and enables single-electron transfer even at zero drain voltage. That operation, however, required an adjustment of the relative phase shift of two ac gate biases, which was somewhat complicated.¹⁷⁾ The turnstile, on the other hand, operates in a single-electron tunneling state with a nonzero drain voltage, but requires only a simple phase shift of π ,^{4,18)} which can be generated by a simpler circuit.

The detailed procedure for single-electron transfer is schematically illustrated in Fig. 2(b). We also show in Fig. 2(a) the potential diagram in an ordinary SET mode for comparison. In the turnstile mode, with a nonzero drain voltage $V_D = (\epsilon_S - \epsilon_D)/e$, where ϵ_S and ϵ_D are the chemical potentials at the source and the drain respectively, we first close channel-2 (See schematic view of Fig. 1.) so that an

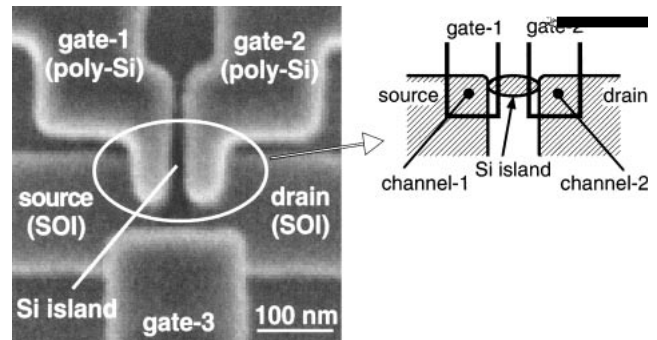


Fig. 1. SEM image and schematic view of the device. Gate-1 and -2 constitute the dual gates for turnstile operations. Gate-3 was not used in this study and its voltage was kept at -1 V throughout the measurements.

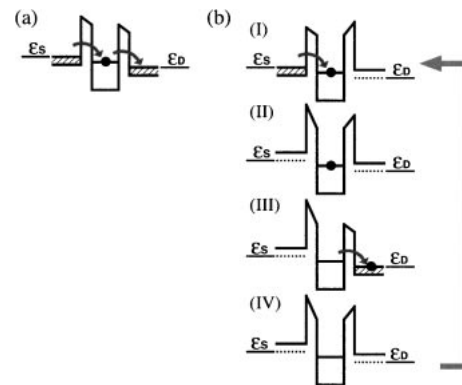


Fig. 2. Potential-profile diagrams for single-electron transfer. In each diagram, ϵ_S , ϵ_D , and the horizontal solid lines beneath them indicate the chemical potentials at the source and drain far from the gates, respectively. (a) Single-electron tunneling of the SET with a nonzero drain voltage, $V_D = (\epsilon_S - \epsilon_D)/e$. Both channels are open, i.e., the conduction-band edge in both channels is below the chemical potential. (b) Sequence for the single-electron turnstile. In each step [(I)–(IV)], at least one of the channel is closed, i.e., the conduction-band edge in the channel(s) is above the chemical potential (schematically shown by the dotted lines).

electron enters only from channel-1 [Figs. 2(b)–(I)]. We next close both channels (II), and then open channel-2 so that an electron emits there (III). Finally, we again close both channels (IV), and open channel-1 (I). This procedure can be accomplished by applying an ac bias to each gate with the phase shift of π . Noteworthy is that, in this turnstile procedure, at least one of the channels is always closed, which was not the case in our previous pump operation.¹⁷⁾

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This is advantageous because high resistance effectively prevents cotunneling,¹⁹⁾ one of the major error sources for electron transfer.

The device was fabricated on a silicon-on-insulator (SOI) substrate. For the fabrication, we used a method we call vertical pattern-dependent oxidation.^{11,14)} This method applies thermal oxidation to a vertically-modulated SOI wire and makes an island automatically in a controlled way. After the island formation, we defined the dual gates, which are made of phosphorus-doped poly-Si (Fig. 1). Next, we again deposited phosphorus-doped poly-Si and defined a broad gate, which covers the entire pattern shown in Fig. 1. That broad gate, called the top gate, is used to generate electron channels outside the dual-gate SET. For the present study, we used the same device that we used in the previous pump study.¹⁷⁾

The measurements were carried out at 25 K. We first characterized the device by dc measurements. Figure 3 shows the gray-scale image of the drain current for the drain voltage of 4 mV in the two gate-voltage (V_{G1} , V_{G2}) plane. The brightest and darkest regions correspond to the drain currents of 1×10^{-10} and 1×10^{-15} A, respectively. V_{G1} and V_{G2} indicate dc voltages applied to gate-1 and -2, respectively. The top gate voltage was kept at 4 V. Black-and-white stripes correspond to the Coulomb blockade oscillation. One can see that the white regions, which indicate the nonvanishing conductance regions, are terminated at both sides. This is because of the closure of the channels. The threshold voltages, V_{th-1} and V_{th-2} , of the channels are around -0.4 V and 0.2 V, respectively, and they are slightly dependent on the voltage of their twin gate because of crosstalk. Notice that the closure of the channel(s) resulted in a very high ($10^{13} \Omega$ or larger) resistance, which is sufficiently high to prevent

cotunneling from flowing during the turnstile operations. The total capacitance (C_{Σ}) and the charging energy ($e^2/2C_{\Sigma}$) of the island were estimated to be 5.4 aF and 15 meV, respectively.

For the turnstile operation, an ac bias was output from a pulse generator, and the amplitude and phase of the transmitted voltage were monitored using an oscilloscope. The measurement setup and the transmitted voltages are shown in Fig. 4. The ac voltages have a phase shift of π , and thus their trajectory in the gate-voltage plane becomes a straight line. The actual trajectory is indicated by the bold white line in Fig. 3. This trajectory follows the electron transfer sequence shown in Fig. 2(b), i.e., it is in the voltage area where at least one of the channels is always closed.

We should mention that, although no current flows around the voltage trajectory shown in Fig. 3, there indeed exists around it electronic states necessary for electron transfer. These states cannot be observed in the dc measurements simply because of the closure of the channel(s) attached to the island. The existence of these states can be confirmed by changing the top gate voltage, which was always fixed at 4 V during ac measurements for turnstile operations. Capacitive coupling of the top gate to the channels and to the island is different, and thus change in the top-gate voltage results in change in the relative position of the threshold lines (V_{th-1} and V_{th-2}) to the Coulomb-blockade oscillation peaks. In fact, by decreasing the top-gate voltage from 4 to 3 V, two current peaks emerged¹⁷⁾ (because the coupling to the island is larger than that to the channels) and further decrease resulted in the emergence of no additional peaks. The present turnstile operation was performed in the dual-gate voltage range near the first one of the two (hidden) peaks.

Figure 5 shows the drain-current versus drain-voltage curves in the yBww13aotined turnstile mode at frequencies of 0.001, 0.5 and 1.0 MHz. Staircases quantized in units of ef are observed for both positive and negative drain voltages. This is clear evidence of single-electron transfer per gate-voltage cycle. The levels of the current plateaus for the positive drain voltages are exactly equal to ef within the accuracy of the present measurement system ($\sim 10^{-2}$). In more detail, for the positive drain voltages, the width of the plateaus is 20–30 mV, which is consistent with the charging energy (15 meV) estimated from the dc measurements; over that width, the plateaus are flat within the uncertainty of the present measurement system ($\sim 10^{-2}$). However, for the negative drain voltages, the levels are slightly larger than $|ef|$. This deviation is due to the unwanted opening of the

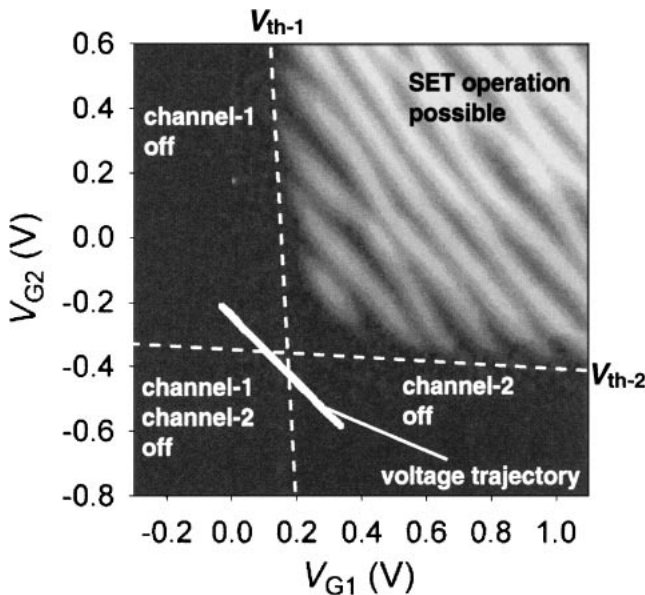


Fig. 3. Gray-scale image of the drain current in the gate-voltage (V_{G1} , V_{G2}) plane in a logarithmic scale. The top-gate voltage and the drain voltage were 4 V and 4 mV, respectively. The measurement temperature was 25 K. The brightest and darkest regions correspond to the drain currents of

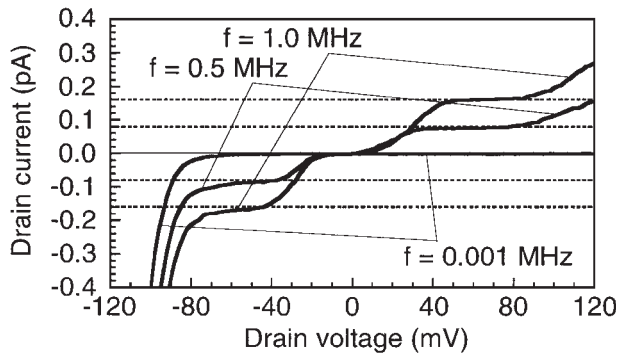


Fig. 5. Drain current as a function of drain voltage for gate-voltage frequencies f of 0.001, 0.5 and 1.0 MHz. Solid curves are the measurement data and the dotted horizontal lines are the quantized levels, i.e., $I = \pm ef$ ($= \pm 160$ fA for $f = 1.0$ MHz and ± 80 fA for $f = 0.5$ MHz). The measurement temperature was 25 K.

channels as a result of the large negative drain voltage reducing the effective gate voltage. This leakage current is added to the turnstile current.

The present operational temperature (25 K) is much higher ($\sim 10^3$) than those in the previous turnstiles using the Al/ Al_2O_3 ³⁾ and GaAs/AlGaAs⁴⁾ structures. The high-temperature operation relies on the small (5.4 aF) total capacitance of the island, which suggests that we can use the turnstile without needing the elaborate cryogenic equipment required by the previous turnstiles.

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- 1) D. J. Thouless: Phys. Rev. B **27** (1983) 6083.
- 2) P. Delsing, K. K. Likharev, L. S. Kuzmin and T. Claeson: Phys. Rev. Lett. **63** (1989) 1861.
- 3) L. J. Geerligs, V. F. Anderegg, P. A. M. Holweg, J. E. Mooij, H. Pothier, D. Esteve, C. Urbina and M. H. Devoret: Phys. Rev. Lett. **64** (1990) 2691.
- 4) L. P. Kouwenhoven, A. T. Johnson, N. C. van der Vaart, C. J. P. M. Harmans and C. T. Foxon: Phys. Rev. Lett. **67** (1991) 1626.
- 5) H. Pothier, P. Lafarge, P. F. Orfila, C. Urbina, D. Esteve and M. H. Devoret: Physica B **169** (1991) 573.
- 6) J. M. Shilton, V. I. Talyanskii, M. Pepper, D. A. Ritchie, J. E. F. Frost, C. J. B. Ford, C. G. Smith and G. A. C. Jones: J. Phys.: Condens. Matter **8** (1996) L531.
- 7) A. Fujiwara and Y. Takahashi: Nature **410** (2001) 560.
- 8) D. V. Averin and K. K. Likharev: J. Low Temp. Phys. **62** (1986) 345.
- 9) T. A. Fulton and G. J. Dolan: Phys. Rev. Lett. **59** (1987) 109.
- 10) Y. Takahashi, H. Namatsu, K. Kurihara, K. Iwadata, M. Nagase and K. Murase: IEEE Trans. Electron Devices **43** (1996) 1213.
- 11) Y. Ono, Y. Takahashi, K. Yamazaki, M. Nagase, H. Namatsu, K. Kurihara and K. Murase: IEEE Trans. Electron Devices **47** (2000) 147.
- 12) M. Saitoh, N. Takahashi, H. Ishikuro and T. Hiramoto: Jpn. J. Appl. Phys. **40** (2001) 2010.
- 13) N. M. Zimmerman, W. H. Huber, A. Fujiwara and Y. Takahashi: Appl. Phys. Lett. **79** (2001) 3188.
- 14) Y. Ono, K. Yamazaki and Y. Takahashi: IEICE Trans. Electron. **E84-C** (2001) 1061.
- 15) A. Fujiwara, S. Horiguchi, M. Nagase and Y. Takahashi: Jpn. J. Appl. Phys. **42** (2003) 2429.
- 16) Y. Takahashi, A. Fujiwara, K. Yamazaki, H. Namatsu, K. Kurihara and K. Murase: Appl. Phys. Lett. **76** (2000) 637.
- 17) Y. Ono and Y. Takahashi: Appl. Phys. Lett. **82** (2003) 1221.
- 18) A. A. Odintsov: Appl. Phys. Lett. **58** (1991) 2695.
- 19) D. V. Averin and Yu. V. Nazarov: Phys. Rev. Lett. **65** (1990) 2446.